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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,551	11/09/2005	Kazuya Hirayanagi	XA-10259	9150

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
02/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
sstiles@milesstockbridge.com

Office Action Summary	Application No.	Applicant(s)	
	10/521,551	HIRAYANAGI ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 371, which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/09/2005 was considered by the examiner.

Drawings

3. The drawings filed on 01/19/2005 were accepted by the examiner.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant by "native instruction of a return processing of returning a program counter of the CPU to a head of the predetermined address space assigned to the execution of the virtual machine instruction at an end thereof." The examiner is not certain what the native instruction of a return processing is accomplishing in the data processing apparatus.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-6, 11-12, and 16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding Claims 1 and 16, the claimed limitations are drawn to workings of an execution routine, representing a program per se, thus constituting non-statutory subject matter since the claim represents actions performed by software.

Regarding Claim 2, the claimed limitations are drawn to an address converting unit whose operation is accomplished through the execution routine of claim 1, thus representing a program per se and constituting non-statutory subject matter. This claim represents actions performed by software.

Regarding Claim 3, the claimed limitations are drawn to the prescribed condition of claim 1 which is part of the workings of the execution routine, thus representing a program per se and constituting non-statutory subject matter. This claim represents actions performed by software.

Regarding Claim 4, the claimed limitations are drawn to a predetermined address that is assigned to a virtual machine instruction, wherein the virtual machine instruction represents a program per se, thus constituting non-statutory subject matter. This claim represents actions performed by software.

Regarding Claim 5, the claimed limitations are drawn to the workings of an execution routine, representing a program per se, thus constituting non-statutory subject matter since the claim represents actions performed by software.

Regarding Claim 6, the claimed limitations are drawn to the workings of an execution routine, a virtual machine instruction, and a conversion table, all representing the workings of a program per se, thus constituting non-statutory subject matter since the claim represents actions performed by software.

Regarding Claims 11 and 12, the claimed limitations are drawn to the workings of an execution routine, a virtual machine instruction, and an address converting unit, all representing the workings of a program per se, thus constituting non-statutory subject matter since the claim represents actions performed by software.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traut (US 6,651,132) in view of Yamahata et al. (4,847,748).

Regarding Claim 1, Traut discloses a data processing apparatus capable of implementing an execution of a virtual machine instruction based on an execution routine specified by a native instruction of a CPU (virtual machine emulated on CPU by the execution of an emulator program, Col. 2, lines 15-36), comprising:

an address converting unit capable of sequentially converting an address output from the CPU into an address of the native instruction by utilizing an address of a prepared execution routine in response to an application of a prescribed condition (page table relates logical memory

addresses to physical memory addresses in response to programs operating in a virtual memory system accessing data locations according to their virtual memory address, the virtual memory address must be translated to a physical memory address to complete read or write operations, Col. 2, lines 52-65), the address converting unit reading a virtual machine instruction to be executed next (read or write access by program operating in virtual memory) and preparing an address of an execution routine corresponding thereto (by performing the translation).

Traut does not teach the address converting unit reading a virtual machine instruction to be executed next and preparing an address of an execution routine corresponding thereto **in parallel** with an execution of the execution routine by the CPU based on the address of the native instruction which is sequentially converted. Yamahata et al. discloses the use of an instruction decoding unit capable of executing an instruction decoding and execution in parallel under virtual memory management (Col. 2, lines 50-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Traut to include the parallel processing of Yamahata since doing so improves performance by shortening the time period for decoding the instruction (Col. 2, line 46-47, and line 54-55).

Regarding Claim 2, Traut in view of Yamahata discloses the data processing apparatus wherein the address converting unit exactly outputs an address input from the CPU in response to a non-application of the prescribed condition (page table relates logical memory addresses to physical memory addresses in response to programs operating in a virtual memory system accessing data locations according to their virtual memory address, Col. 2, lines 52-65. Therefore, non-application of the condition represents an access by a program that is not

operating in virtual memory, thus translation is not necessary and the CPU address is left unchanged).

Regarding Claim 3, Traut in view of Yamahata discloses the data processing apparatus wherein the prescribed condition is an output of a predetermined address by the CPU (page table relates logical memory addresses to physical memory addresses in response to programs operating in a virtual memory system accessing data locations according to their virtual memory address, Col. 2, lines 52-65. Therefore, the condition is the access of a program operating in virtual memory, thus representing an output of a predetermined address in virtual format).

Regarding Claim 4, Traut in view of Yamahata discloses the data processing apparatus wherein the predetermined address is a starting address of a predetermined address space assigned to the execution of the virtual machine instruction (page table relates logical memory addresses to physical memory addresses in response to programs operating in a virtual memory system accessing data locations according to their virtual memory address, Col. 2, lines 52-65, wherein the address represents the address for the access which points to the start of a virtual address space to be accessed).

Regarding Claim 5, The Traut in view of Yamahata discloses the data processing apparatus wherein the execution routine includes a native instruction of a return processing of returning a program counter of the CPU to a head of the predetermined address space assigned to the execution of the virtual machine instruction at an end thereof (first counter means adapted to be counted up in response to the effective address computation requiring signal and down in response to the translation completion signal, Yamahata, Col. 3, lines 14-26).

Regarding Claim 6, Traut in view of Yamahata discloses the data processing apparatus further comprising a conversion table for defining a correspondence of an instruction length to an address of an execution routine for each virtual machine instruction (page table relates logical memory addresses of a particular length to physical memory addresses, Traut, Col. 2, lines 52-55).

Regarding Claim 11, Traut in view of Yamahata discloses the data processing apparatus wherein when a virtual machine instruction which is read is a branch instruction, the address converting unit can read a virtual machine instruction of a branch destination and can prepare an address of an execution routine corresponding thereto (translation exception such as a page fault, representing a branch instructions, is detected for the translation to the virtual address into a real address, Col. 5, lines 1-8).

Regarding Claim 12, Traut in view of Yamahata discloses the data processing apparatus wherein when a virtual machine instruction which is read is a conditional branch instruction, the address converting unit further reads a virtual machine instruction of a branch destination and separately prepares an address of an execution routine corresponding thereto, and selects an address of an execution routine to be utilized for an address conversion depending on a presence of a branch (translation exception such as a page fault, representing a branch instructions, is detected for the translation to the virtual address into a real address, Col. 5, lines 1-8 wherein the condition is the request from the instruction code unit 2).

Regarding Claim 13, Traut in view of Yamahata discloses the data processing apparatus further comprising a first memory for storing a virtual machine program constituted by a virtual machine instruction (Traut, long term storage such as hard disks, Col. 2, lines 37-51) and a

second memory for storing an execution routine thereof for each virtual machine instruction (Traut, dynamic RAM, Col. 2, lines 37-51), the data processing apparatus being formed on a semiconductor chip (the invention is formed within a microprocessor, Figure 3, Yamahata, thus representing a single chip).

Regarding Claim 14, Traut in view of Yamahata discloses the data processing apparatus wherein the second memory further has an instruction length of a virtual machine instruction (dynamic RAM accommodates the size of the virtual address space, Col. 2, lines 37-51).

Regarding Claim 15, Traut in view of Yamahata discloses the data processing apparatus wherein the first memory is a rewritable non-volatile memory (disk drives, Col. 2, lines 37-51).

Claim 16 is rejected using the same rationale as that of Claim 1, wherein the invention is formed within a microprocessor (Figure 3, Yamahata) thus representing a single IC card (or chip) having an input/output circuit (instructions are inputted to instruction queue 1 and outputted by the system either to the bus interface, from the address translation unit 4, or to the instruction execution unit 7, see Figure 3) and a data processing apparatus connected to the input/output circuit on a card board (instruction execution unit 7).

10. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traut (US 6,651,132) in view of Yamahata et al. (4,847,748) as applied to claims 1-6 above, and further in view of Liokumovich et al. (US 2003/0115578).

Regarding Claim 7, Traut in view of Yamahata discloses the data processing apparatus further comprising a first register for holding an address of an execution routine which is acquired (Yamahata, effective address register 8 acquired from the address computation unit 3, see Col. 9, lines 39-46). Traut in view of Yamahata does not teach a second register for holding

an instruction length acquired from the conversion table corresponding to a virtual machine instruction. Liokumovich et al. discloses the use of segment registers to hold descriptor values related to the base and size of the translated code (Page 2, paragraphs 0024-0027). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Traut in view of Yamahata to include the use of segment registers, as shown by Liokumovich, since these facilitate seamless maintenance of descriptor tables for virtual systems.

Regarding Claim 8, Traut in view of Yamahata further in view of Liokumovich discloses the data processing apparatus wherein the address converting unit has a virtual machine program counter for outputting an address to read a virtual machine instruction from a memory (count up or counting down of program counter, Col. 5, line 50 - Col. 8, line 8) and an amount of an increment of the virtual machine program counter can be controlled based on a value of the first register (Col. 9, line 17-46, effective address register, Yamahata).

Regarding Claim 9, Traut in view of Yamahata further in view of Liokumovich discloses the data processing apparatus wherein the increment of the virtual machine program counter is carried out synchronously with an execution end timing of an execution routine (incrementing the counter, Col. 5, lines 50-65, Yamahata).

Regarding Claim 10, Traut in view of Yamahata further in view of Liokumovich discloses the data processing apparatus wherein the address converting unit has an execution routine address generating circuit (address computation unit 3) for reading a native instruction of an execution routine from a memory (instruction form instruction queue 1 is decoded by instruction decoder 2), and the execution routine address generating circuit has a third register for inputting an address of an execution routine held by the second register and an adder for

adding a value of the third register to a plurality of bits on a low order side of an address output from the CPU, and an output of the adder is set to be an address of a native instruction of an execution routine (CPU calculates the linear address by adding the offset to a segment base and checks all protection conditions, Page 2, paragraph 0023, Liokumovich).

The examine would like to note that claims 1-16 contain "intended use" functionality language such as: "data processing apparatus **capable of** implementing...", "address converting unit **capable of** sequentially converting...", "conversion table **for** defining...", "register **for** holding...", "counter **for** outputting...", "counter **can be** controlled...", "address generating circuit **for** reading...", and "processing apparatus **can implement** an execution..." (among other occurrences within the claims).

Applicant is advised that "intended use" language in the claims does not add any patentable weight. If applicant's intention is to claim the functional language, applicant is advised to change the limitations to positively claim these functions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-TH 6:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Midys Rojas
Examiner
Art Unit 2185

MR

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100